

METHOD AND CIRCUIT FOR OPTIMIZING POWER EFFICIENCY IN A DC-DC CONVERTER

5

Abstract of the Disclosure

In one embodiment, a turn-on delay control structure (30) includes a sense FET device (31) that is coupled to a switch node (13) in a synchronous DC-DC converter (10). The DC-DC converter includes a high-side switch (11) and a low-side switch (12). The sense FET device (31) senses current conduction in a body diode (18) of the low-side switch (12). A current sensing/comparator circuit (32) coupled to the sense FET (31) detects changes in current conduction. A delay circuit (33) and a clock/logic circuit (32) coupled to the current sensing/comparator circuit (32) predict and adjust delay time in switching between the high-side switch (11) and the low-side switch (12).